



# TEA5767HN

Low-power FM stereo radio for handheld applications

Rev. 05 — 26 January 2007

Product data sheet

## 1. General description

---

The TEA5767HN is a single-chip electronically tuned FM stereo radio for low-voltage applications with fully integrated Intermediate Frequency (IF) selectivity and demodulation. The radio is completely adjustment-free and only requires a minimum of small and low cost external components. The radio can be tuned to the European, US, and Japanese FM bands.

## 2. Features

---

- High sensitivity due to integrated low-noise RF input amplifier
- FM mixer for conversion to IF of the US/Europe (87.5 MHz to 108 MHz) and Japanese (76 MHz to 91 MHz) FM band
- Preset tuning to receive Japanese TV audio up to 108 MHz
- RF Automatic Gain Control (AGC) circuit
- LC tuner oscillator operating with low cost fixed chip inductors
- FM IF selectivity performed internally
- No external discriminator needed due to fully integrated FM demodulator
- Crystal reference frequency oscillator; the oscillator operates with a 32.768 kHz clock crystal or with a 13 MHz crystal and with an externally applied 6.5 MHz reference frequency
- Phase-locked loop (PLL) synthesizer tuning system
- I<sup>2</sup>C-bus and 3-wire bus, selectable via pin BUSMODE
- 7-bit IF counter output via the bus
- 4-bit level information output via the bus
- Soft mute
- Signal dependent mono to stereo blend [Stereo Noise Cancelling (SNC)]
- Signal dependent High Cut Control (HCC)
- Soft mute, SNC and HCC can be switched off via the bus
- Adjustment-free stereo decoder
- Autonomous search tuning function
- Standby mode
- Two software programmable ports
- Bus enable line to switch the bus input and output lines into 3-state mode

### 3. Quick reference data

**Table 1. Quick reference data**

$V_{CCA} = V_{CCD} = V_{CC(VCO)} = 2.7\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; AC values are given in RMS; for  $V_{RF}$  the emf value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CCA}$	analog supply voltage		[1] 2.5	3.0	5.0	V
$V_{CC(VCO)}$	Voltage-Controlled Oscillator (VCO) supply voltage		[1] 2.5	3.0	5.0	V
$V_{CCD}$	digital supply voltage		[1] 2.5	3.0	5.0	V
$I_{CCA}$	analog supply current	operating; $V_{CCA} = 3\text{ V}$	6.0	8.4	10.5	mA
		Standby mode; $V_{CCA} = 3\text{ V}$	-	3	6	$\mu\text{A}$
$I_{CC(VCO)}$	VCO supply current	operating; $V_{CC(VCO)} = 3\text{ V}$	560	750	940	$\mu\text{A}$
		Standby mode; $V_{CC(VCO)} = 3\text{ V}$	-	1	2	$\mu\text{A}$
$I_{CCD}$	digital supply current	operating; $V_{CCD} = 3\text{ V}$	2.1	3.0	3.9	mA
		Standby mode; $V_{CCD} = 3\text{ V}$				
		bus enable line HIGH	30	56	80	$\mu\text{A}$
	bus enable line LOW	11	19	26	$\mu\text{A}$	
$f_{FM(ant)}$	FM input frequency		76	-	108	MHz
$T_{amb}$	ambient temperature	$V_{CCA} = V_{CC(VCO)} = V_{CCD} = 2.5\text{ V to }5\text{ V}$	-10	-	+75	$^\circ\text{C}$
<b>FM overall system parameters; see Figure 13</b>						
$V_{RF}$	RF sensitivity input voltage	$f_{RF} = 76\text{ MHz to }108\text{ MHz}$ ; $\Delta f = 22.5\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; (S+N)/N = 26 dB; de-emphasis = 75 $\mu\text{s}$ ; L = R; $B_{AF} = 300\text{ Hz to }15\text{ kHz}$	-	2	3.5	$\mu\text{V}$
$S_{-200}$	low side 200 kHz selectivity	$\Delta f = -200\text{ kHz}$ ; $f_{tune} = 76\text{ MHz to }108\text{ MHz}$	[2] 32	36	-	dB
$S_{+200}$	high side 200 kHz selectivity	$\Delta f = +200\text{ kHz}$ ; $f_{tune} = 76\text{ MHz to }108\text{ MHz}$	[2] 39	43	-	dB
$V_{AFL}$	left audio frequency output voltage	$V_{RF} = 1\text{ mV}$ ; L = R; $\Delta f = 22.5\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; de-emphasis = 75 $\mu\text{s}$	60	75	90	mV
$V_{AFR}$	right audio frequency output voltage	$V_{RF} = 1\text{ mV}$ ; L = R; $\Delta f = 22.5\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; de-emphasis = 75 $\mu\text{s}$	60	75	90	mV

**Table 1. Quick reference data ...continued**

$V_{CCA} = V_{CCD} = V_{CC(VCO)} = 2.7\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; AC values are given in RMS; for  $V_{RF}$  the emf value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
(S+N)/N	maximum signal plus noise-to-noise ratio	$V_{RF} = 1\text{ mV}$ ; $L = R$ ; $\Delta f = 22.5\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; de-emphasis = $75\text{ }\mu\text{s}$ ; $B_{AF} = 300\text{ Hz to }15\text{ kHz}$	54	60	-	dB
$\alpha_{CS(stereo)}$	stereo channel separation	$V_{RF} = 1\text{ mV}$ ; $R = L = 0$ or $R = 0$ and $L = 1$ including 9 % pilot; $\Delta f = 75\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; data byte 3 bit 3 = 0; data byte 4 bit 1 = 1	24	30	-	dB
THD	total harmonic distortion	$V_{RF} = 1\text{ mV}$ ; $L = R$ ; $\Delta f = 75\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; de-emphasis = $75\text{ }\mu\text{s}$	-	0.4	1	%

[1]  $V_{CCA}$ ,  $V_{CC(VCO)}$  and  $V_{CCD}$  must not differ by more than 200 mV.

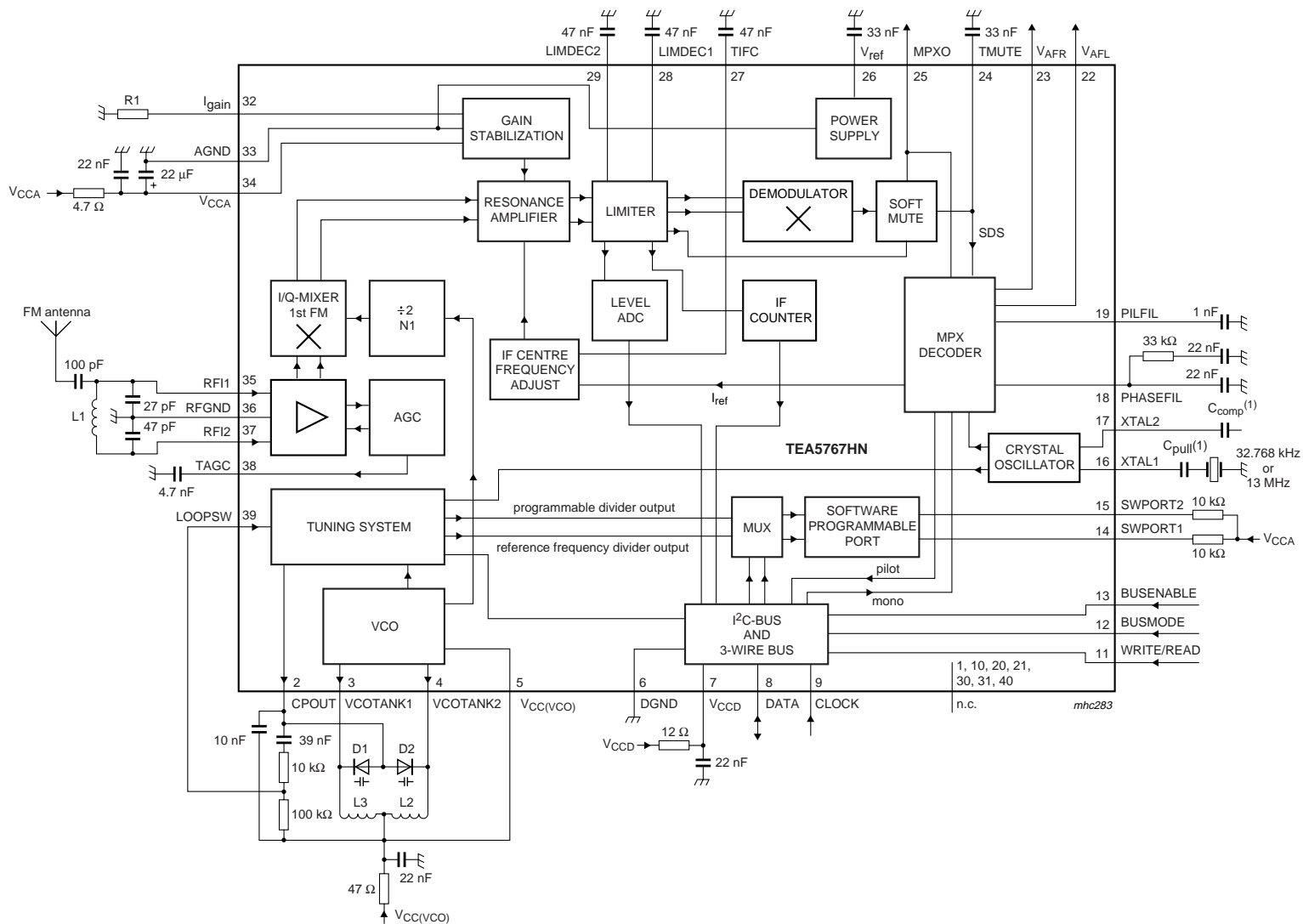
[2] Low side and high side selectivity can be switched by changing the mixer from high side to low side LO injection.

## 4. Ordering information

**Table 2. Ordering information**

Type number	Package		
	Name	Description	Version
TEA5767HN	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body $6 \times 6 \times 0.85\text{ mm}$	SOT618-1

5. Block diagram



The component list is given in [Section 16](#).

(1)  $C_{comp}$  and  $C_{pull}$  data depends on crystal specification.

Fig 1. Block diagram

## 6. Pinning information

### 6.1 Pinning

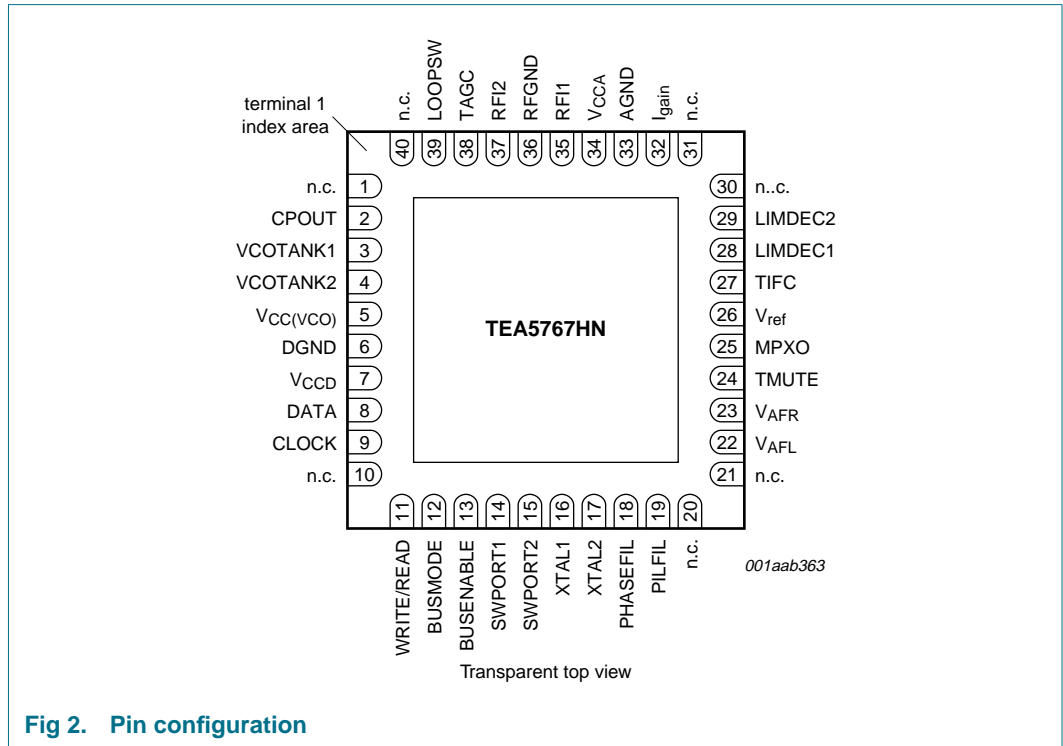


Fig 2. Pin configuration

### 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
CPOUT	2	charge pump output of synthesizer PLL
VCOTANK1	3	VCO tuned circuit output 1
VCOTANK2	4	VCO tuned circuit output 2
V <sub>CC(VCO)</sub>	5	VCO supply voltage
DGND	6	digital ground
V <sub>CCD</sub>	7	digital supply voltage
DATA	8	bus data line input/output
CLOCK	9	bus clock line input
n.c.	10	not connected
WRITE/READ	11	write/read control input for the 3-wire bus
BUSMODE	12	bus mode select input
BUSENABLE	13	bus enable input
SWPORT1	14	software programmable port 1
SWPORT2	15	software programmable port 2
XTAL1	16	crystal oscillator input 1

Table 3. Pin description ...continued

Symbol	Pin	Description
XTAL2	17	crystal oscillator input 2
PHASEFIL	18	phase detector loop filter
PILFIL	19	pilot detector low-pass filter
n.c.	20	not connected
n.c.	21	not connected
V <sub>AFL</sub>	22	left audio frequency output voltage
V <sub>AFR</sub>	23	right audio frequency output voltage
TMUTE	24	time constant for soft mute
MPXO	25	FM demodulator MPX signal output
V <sub>ref</sub>	26	reference voltage
TIFC	27	time constant for IF center adjust
LIMDEC1	28	decoupling IF limiter 1
LIMDEC2	29	decoupling IF limiter 2
n.c.	30	not connected
n.c.	31	not connected
I <sub>gain</sub>	32	gain control current for IF filter
AGND	33	analog ground
V <sub>CCA</sub>	34	analog supply voltage
RFI1	35	RF input 1
RFGND	36	RF ground
RFI2	37	RF input 2
TAGC	38	time constant RF AGC
LOOPSW	39	switch output of synthesizer PLL loop filter
n.c.	40	not connected

## 7. Functional description

### 7.1 Low-noise RF amplifier

The Low Noise Amplifier (LNA) input impedance together with the LC RF input circuit defines an FM band filter. The gain of the LNA is controlled by the RF AGC circuit.

### 7.2 FM mixer

The FM quadrature mixer converts the FM RF (76 MHz to 108 MHz) to an IF of 225 kHz.

### 7.3 VCO

The varactor tuned LC VCO provides the Local Oscillator (LO) signal for the FM quadrature mixer. The VCO frequency range is 150 MHz to 217 MHz.

## 7.4 Crystal oscillator

The crystal oscillator can operate with a 32.768 kHz clock crystal or a 13 MHz crystal. The temperature drift of standard 32.768 kHz clock crystals limits the operational temperature range from  $-10\text{ }^{\circ}\text{C}$  to  $+60\text{ }^{\circ}\text{C}$ .

The PLL synthesizer can be clocked externally with a 32.768 kHz, a 6.5 MHz or a 13 MHz signal via pin XTAL2.

The crystal oscillator generates the reference frequency for:

- The reference frequency divider for the synthesizer PLL
- The timing for the IF counter
- The free-running frequency adjustment of the stereo decoder VCO
- The center frequency adjustment of the IF filters

## 7.5 PLL tuning system

The PLL synthesizer tuning system is suitable to operate with a 32.768 kHz or a 13 MHz reference frequency generated by the crystal oscillator or applied to the IC from an external source. The synthesizer can also be clocked via pin XTAL2 at 6.5 MHz. The PLL tuning system can perform an autonomous search tuning function.

## 7.6 RF AGC

The RF AGC prevents overloading and limits the amount of intermodulation products created by strong adjacent channels.

## 7.7 IF filter

Fully integrated IF filter.

## 7.8 FM demodulator

The FM quadrature demodulator has an integrated resonator to perform the phase shift of the IF signal.

## 7.9 Level voltage generator and analog-to-digital converter

The FM IF analog level voltage is converted to 4 bits digital data and output via the bus.

## 7.10 IF counter

The IF counter outputs a 7-bit count result via the bus.

## 7.11 Soft mute

The low-pass filtered level voltage drives the soft mute attenuator at low RF input levels. The soft mute function can be switched off via the bus.

## 7.12 MPX decoder

The PLL stereo decoder is adjustment-free. The stereo decoder can be switched to mono via the bus.

### 7.13 Signal dependent mono to stereo blend

With a decreasing RF input level the MPX decoder blends from stereo to mono to limit the output noise. The continuous mono to stereo blend can also be programmed via the bus to an RF level depending switched mono to stereo transition. Stereo Noise Cancelling (SNC) can be switched off via the bus.

### 7.14 Signal dependent AF response

The audio bandwidth will be reduced with a decreasing RF input level. This function can be switched off via the bus.

### 7.15 Software programmable ports

Two software programmable ports (open-collector) can be addressed via the bus.

The port 1 (pin SWPORT1) function can be changed with write data byte 4 bit 0 (see [Table 13](#)). Pin SWPORT1 is then output for the ready flag of read byte 1.

### 7.16 I<sup>2</sup>C-bus and 3-wire bus

The 3-wire bus and the I<sup>2</sup>C-bus operate with a maximum clock frequency of 400 kHz.

Before any READ or WRITE operation the pin BUSENABLE has to be HIGH for at least 10  $\mu$ s.

The I<sup>2</sup>C-bus mode is selected when pin BUSMODE is LOW, when pin BUSMODE is HIGH the 3-wire bus mode is selected.



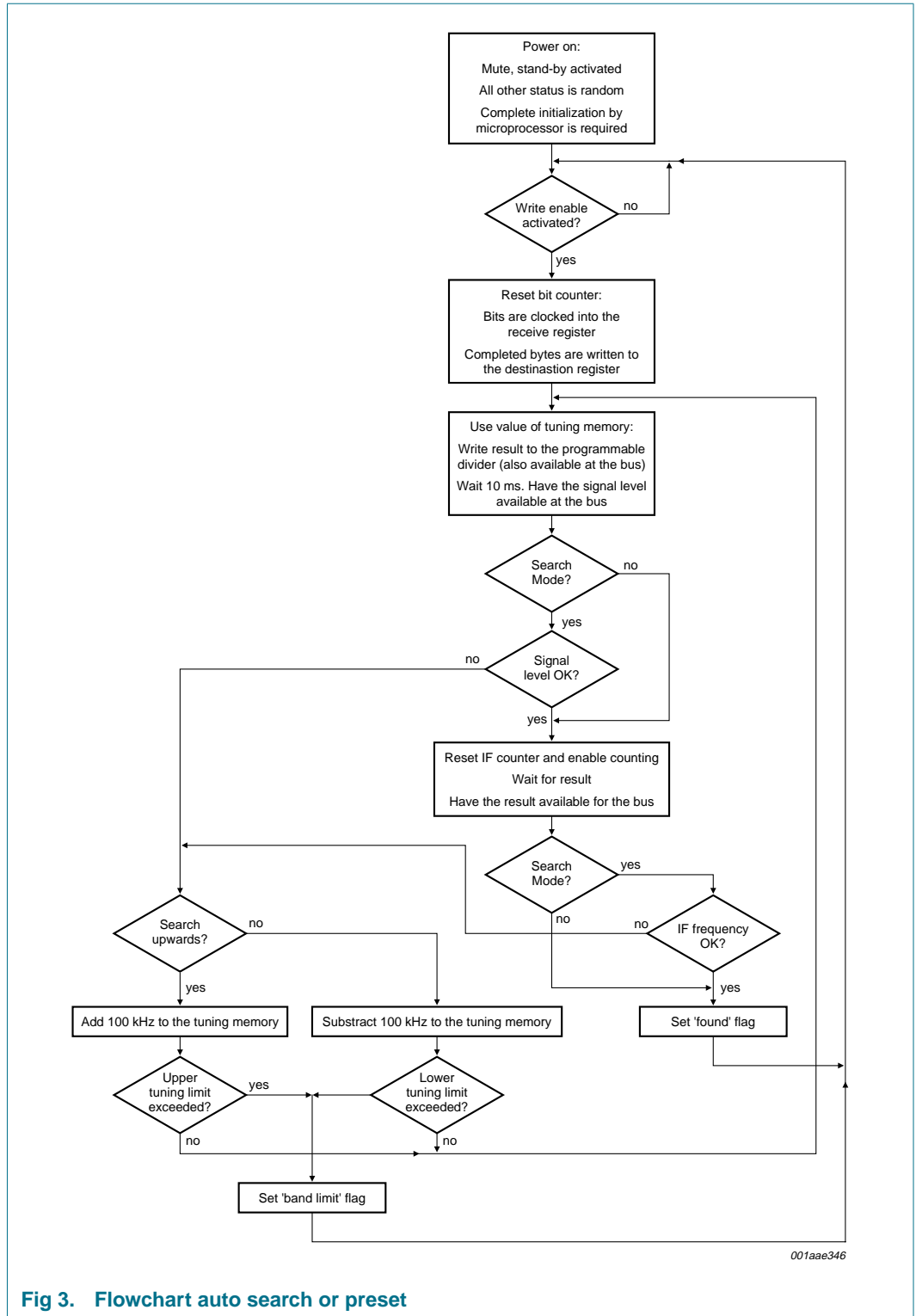


Fig 3. Flowchart auto search or preset

## 8. I<sup>2</sup>C-bus, 3-wire bus and bus-controlled functions

### 8.1 I<sup>2</sup>C-bus specification

Information about the I<sup>2</sup>C-bus can be found in the brochure “*The I<sup>2</sup>C-bus and how to use it*” (order number 9398 393 40011).

The standard I<sup>2</sup>C-bus specification is expanded by the following definitions:

IC address: 110 0000b

Structure of the I<sup>2</sup>C-bus logic: slave transceiver

Subaddresses are not used

The maximum LOW-level input and the minimum HIGH-level input are specified to 0.2V<sub>CCD</sub> and 0.45V<sub>CCD</sub> respectively.

The pin BUSMODE must be connected to ground to operate the IC with the I<sup>2</sup>C-bus.

**Remark:** The I<sup>2</sup>C-bus operates at a maximum clock frequency of 400 kHz. It is not allowed to connect the IC to an I<sup>2</sup>C-bus operating at a higher clock rate.

#### 8.1.1 Data transfer

Data sequence: address, byte 1, byte 2, byte 3, byte 4 and byte 5 (the data transfer has to be in this order). The Least Significant Bit (LSB) = 0 of the address indicates a WRITE operation to the TEA5767HN.

Bit 7 of each byte is considered as the Most Significant Bit (MSB) and has to be transferred as the first bit of the byte.

The data becomes valid bitwise at the appropriate falling edge of the clock. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte is not completed, the new bits will be used, but a new tuning cycle will not be started

The IC can be switched into a low current Standby mode with the standby bit; the bus is then still active. The standby current can be reduced by deactivating the bus interface (pin BUSENABLE LOW). If the bus interface is deactivated (pin BUSENABLE LOW) without the Standby mode being programmed, the IC maintains normal operation, but is isolated from the bus lines.

The software programmable output (SWPORT1) can be programmed to operate as a tuning indicator output. As long as the IC has not completed a tuning action, pin SWPORT1 remains LOW. The pin becomes HIGH, when a preset or search tuning is completed or when a band limit is reached.

The reference frequency divider of the synthesizer PLL is changed when the MSB in byte 5 is set to logic 1. The tuning system can then be clocked via pin XTAL2 at 6.5 MHz.

8.1.2 Power-on reset

At Power-on reset the mute is set, all other bits are set to LOW. To initialize the IC all bytes have to be transferred.

8.2 I<sup>2</sup>C-bus protocol

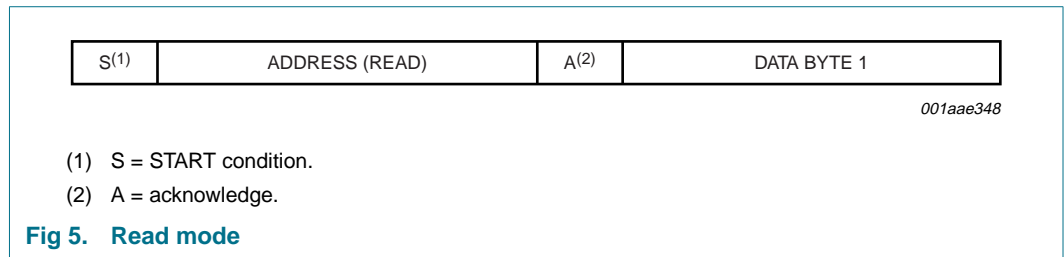
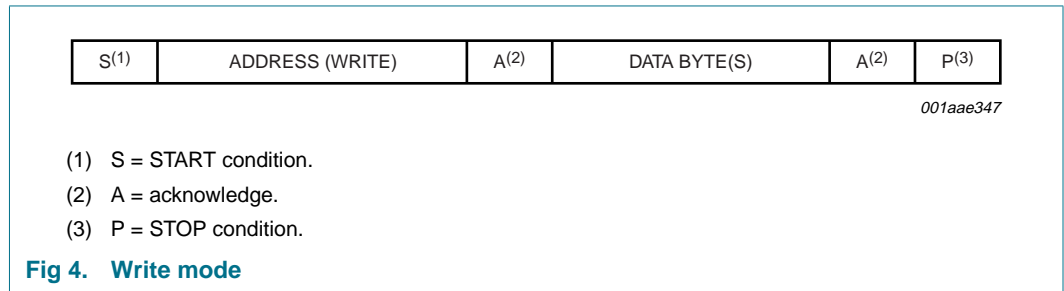
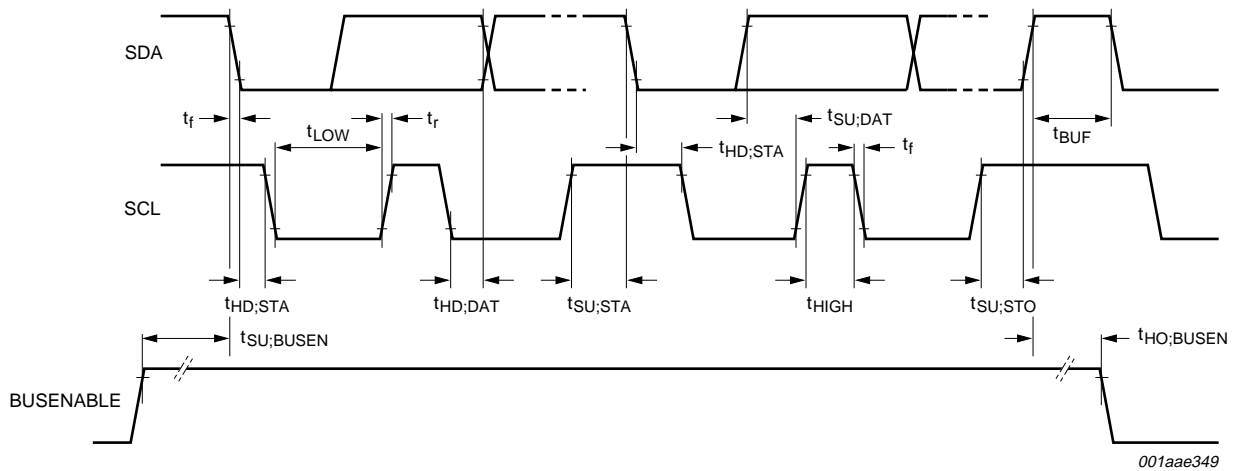


Table 4. IC address byte

IC address							Mode
1	1	0	0	0	0	0	R/W <sup>[1]</sup>

[1] Read or write mode:  
 a) 0 = write operation to the TEA5767HN.  
 b) 1 = read operation from the TEA5767HN.



$t_f$  = fall time of both SDA and SCL signals:  $20 + 0.1C_b < t_f < 300$  ns, where  $C_b$  = capacitive load on bus line in pF.  
 $t_r$  = rise time of both SDA and SCL signals:  $20 + 0.1C_b < t_r < 300$  ns, where  $C_b$  = capacitive load on bus line in pF.  
 $t_{HD,STA}$  = hold time (repeated) START condition. After this period, the first clock pulse is generated:  $> 600$  ns.  
 $t_{HIGH}$  = HIGH period of the SCL clock:  $> 600$  ns.  
 $t_{LOW}$  = LOW period of the SCL clock  $> 1300$  ns.  
 $t_{SU,STA}$  = set-up time for a repeated START condition:  $> 600$  ns.  
 $t_{HD,DAT}$  = data hold time:  $300$  ns  $< t_{HD,DAT} < 900$  ns.  
**Remark:** 300 ns lower limit is added because the ASIC has no internal hold time for the SDA signal.  
 $t_{SU,DAT}$  = data set-up time:  $t_{SU,DAT} > 100$  ns. If ASIC is used in a standard mode I<sup>2</sup>C-bus system,  $t_{SU,DAT} > 250$  ns.  
 $t_{SU,STO}$  = set-up time for STOP condition:  $> 600$  ns.  
 $t_{BUF}$  = bus free time between a STOP and a START condition:  $> 600$  ns.  
 $C_b$  = capacitive load of one bus line:  $< 400$  pF.  
 $t_{SU,BUSEN}$  = bus enable set-up time:  $t_{SU,BUSEN} > 10$   $\mu$ s.  
 $t_{HO,BUSEN}$  = bus enable hold time:  $t_{HO,BUSEN} > 10$   $\mu$ s.

**Remark:** The terms SDA and SCL are the corresponding terms used by the I<sup>2</sup>C-bus for the DATA and CLOCK signals respectively.

Fig 6. I<sup>2</sup>C-bus timing diagram

### 8.3 3-wire bus specification

The 3-wire bus controls the write/read, clock and data lines and operates at a maximum clock frequency of 400 kHz.

**Hint:** By using the standby bit the IC can be switched into a low current Standby mode. In Standby mode the IC must be in the WRITE mode. When the IC is switched to READ mode, during standby, the IC will hold the data line down. The standby current can be reduced by deactivating the bus interface (pin BUSENABLE LOW). If the bus interface is deactivated (pin BUSENABLE LOW) without the Standby mode being programmed, the IC maintains normal operation, but is isolated from the clock and data line.

#### 8.3.1 Data transfer

Data sequence: byte 1, byte 2, byte 3, byte 4 and byte 5 (the data transfer has to be in this order).

A positive edge at pin WRITE/READ enables the data transfer into the IC. The data has to be stable at the positive edge of the clock. Data may change while the clock is LOW and is written into the IC on the positive edge of the clock. Data transfer can be stopped after the transmission of new tuning information with the first two bytes or after each following byte.

A negative edge at pin WRITE/READ enables the data transfer from the IC. The WRITE/READ pin changes while the clock is LOW. With the negative edge at pin WRITE/READ the MSB of the first byte occurs at pin DATA.

The bits are shifted on the negative clock edge to pin DATA and can be read on the positive edge.

To do two consecutive read or write actions, pin WRITE/READ has to be toggled for at least one clock period. When a search tuning request is sent, the IC autonomously starts searching the FM band; the search direction and search stop level can be selected. When a station with a field strength equal to or greater than the stop level is found, the tuning system stops and the ready flag bit is set to HIGH. When, during search, a band limit is reached, the tuning system stops at the band limit and the band limit flag bit is set to HIGH. The ready flag is also set to HIGH in this case.

The software programmable output (SWPORT1) can be programmed to operate as a tuning indicator output. As long as the IC has not completed a tuning action, pin SWPORT1 remains LOW. The pin becomes HIGH, when a preset or search tuning is completed or when a band limit is reached.

The reference frequency divider of the synthesizer PLL is changed when the MSB in byte 5 is set to logic 1. The tuning system can then be clocked via pin XTAL2 at 6.5 MHz.

8.3.2 Power-on reset

At Power-on reset the mute is set, all other bits are random. To initialize the IC all bytes have to be transferred.

8.4 Writing data

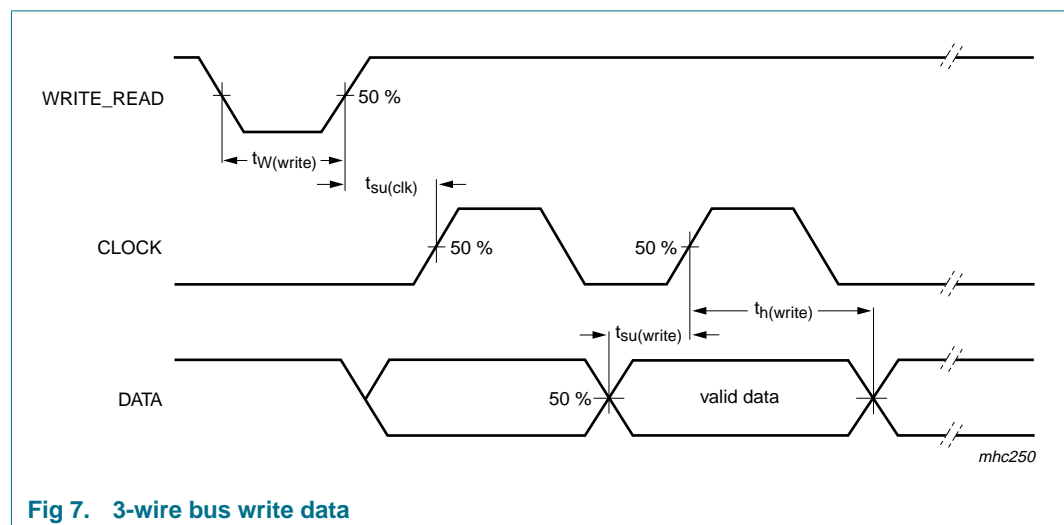


Fig 7. 3-wire bus write data

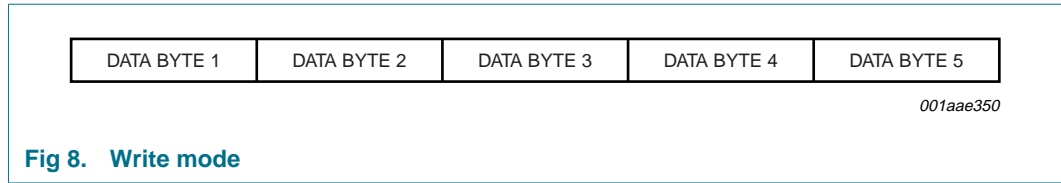


Fig 8. Write mode

Table 5. Format of 1st data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
MUTE	SM	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 6. Description of 1st data byte bits

Bit	Symbol	Description
7	MUTE	if MUTE = 1 then L and R audio are muted; if MUTE = 0 then L and R audio are not muted
6	SM	<b>Search mode:</b> if SM = 1 then in search mode; if SM = 0 then not in search mode
5 to 0	PLL[13:8]	setting of synthesizer programmable counter for search or preset

Table 7. Format of 2nd data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 8. Description of 2nd data byte bits

Bit	Symbol	Description
7 to 0	PLL[7:0]	setting of synthesizer programmable counter for search or preset

Table 9. Format of 3rd data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
SUD	SSL1	SSL0	HLSI	MS	MR	ML	SWP1

Table 10. Description of 3rd data byte bits

Bit	Symbol	Description
7	SUD	<b>Search Up/Down:</b> if SUD = 1 then search up; if SUD = 0 then search down
6 and 5	SSL[1:0]	<b>Search Stop Level:</b> see <a href="#">Table 11</a>
4	HLSI	<b>High/Low Side Injection:</b> if HLSI = 1 then high side LO injection; if HLSI = 0 then low side LO injection
3	MS	<b>Mono to Stereo:</b> if MS = 1 then forced mono; if MS = 0 then stereo ON
2	MR	<b>Mute Right:</b> if MR = 1 then the right audio channel is muted and forced mono; if MR = 0 then the right audio channel is not muted
1	ML	<b>Mute Left:</b> if ML = 1 then the left audio channel is muted and forced mono; if ML = 0 then the left audio channel is not muted
0	SWP1	<b>Software programmable port 1:</b> if SWP1 = 1 then port 1 is HIGH; if SWP1 = 0 then port 1 is LOW

**Table 11. Search stop level setting**

SSL1	SSL0	Search stop level
0	0	not allowed in search mode
0	1	low; level ADC output = 5
1	0	mid; level ADC output = 7
1	1	high; level ADC output = 10

**Table 12. Format of 4th data byte**

7 (MSB)	6	5	4	3	2	1	0 (LSB)
SWP2	STBY	BL	XTAL	SMUTE	HCC	SNC	SI

**Table 13. Description of 4th data byte bits**

Bit	Symbol	Description
7	SWP2	<b>Software programmable port 2:</b> if SWP2 = 1 then port 2 is HIGH; if SWP2 = 0 then port 2 is LOW
6	STBY	<b>Standby:</b> if STBY = 1 then in Standby mode; if STBY = 0 then not in Standby mode
5	BL	<b>Band Limits:</b> if BL = 1 then Japanese FM band; if BL = 0 then US/Europe FM band
4	XTAL	<b>Clock frequency:</b> see <a href="#">Table 16</a>
3	SMUTE	<b>Soft Mute:</b> if SMUTE = 1 then soft mute is ON; if SMUTE = 0 then soft mute is OFF
2	HCC	<b>High Cut Control:</b> if HCC = 1 then high cut control is ON; if HCC = 0 then high cut control is OFF
1	SNC	<b>Stereo Noise Cancelling:</b> if SNC = 1 then stereo noise cancelling is ON; if SNC = 0 then stereo noise cancelling is OFF
0	SI	<b>Search Indicator:</b> if SI = 1 then pin SWPORT1 is output for the ready flag; if SI = 0 then pin SWPORT1 is software programmable port 1

**Table 14. Format of 5th data byte**

7 (MSB)	6	5	4	3	2	1	0 (LSB)
PLLREF	DTC	-	-	-	-	-	-

**Table 15. Description of 5th data byte bits**

Bit	Symbol	Description
7	PLLREF	if PLLREF = 1 then the 6.5 MHz reference frequency for the PLL is enabled; if PLLREF = 0 then the 6.5 MHz reference frequency for the PLL is disabled; see <a href="#">Table 16</a>
6	DTC	if DTC = 1 then the de-emphasis time constant is 75 $\mu$ s; if DTC = 0 then the de-emphasis time constant is 50 $\mu$ s
5 to 0	-	not used; position is don't care

Table 16. Clock bits setting

PLLREF	XTAL	Clock frequency
0	0	13 MHz
0	1	32.768 kHz
1	0	6.5 MHz
1	1	not allowed

8.5 Reading data

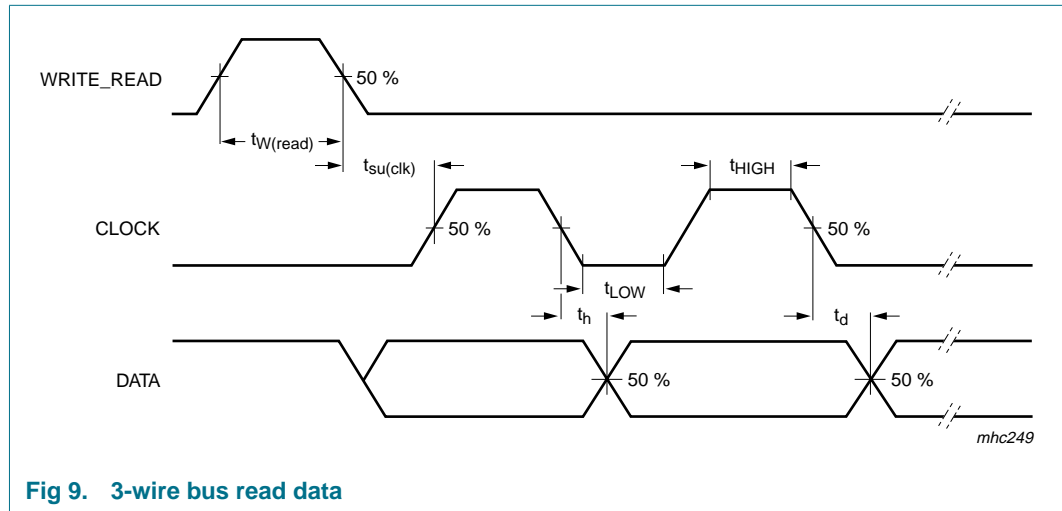


Fig 9. 3-wire bus read data

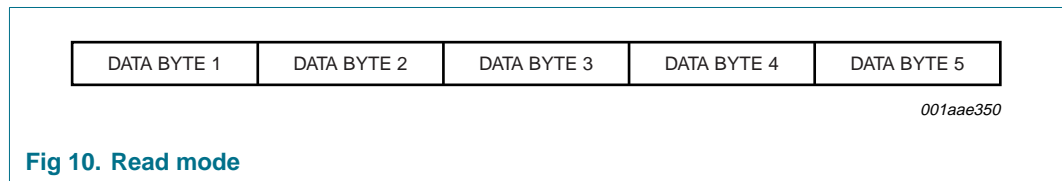


Fig 10. Read mode

Table 17. Format of 1st data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
RF	BLF	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 18. Description of 1st data byte bits

Bit	Symbol	Description
7	RF	<b>Ready Flag:</b> if RF = 1 then a station has been found or the band limit has been reached; if RF = 0 then no station has been found
6	BLF	<b>Band Limit Flag:</b> if BLF = 1 then the band limit has been reached; if BLF = 0 then the band limit has not been reached
5 to 0	PLL[13:8]	setting of synthesizer programmable counter after search or preset

Table 19. Format of 2nd data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0



Table 20. Description of 2nd data byte bits

Bit	Symbol	Description
7 to 0	PLL[7:0]	setting of synthesizer programmable counter after search or preset

Table 21. Format of 3rd data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
STEREO	IF6	IF5	IF4	IF3	IF2	IF1	IF0

Table 22. Description of 3rd data byte bits

Bit	Symbol	Description
7	STEREO	<b>Stereo indication:</b> if STEREO = 1 then stereo reception; if STEREO = 0 then mono reception
6 to 0	PLL[13:8]	IF counter result

Table 23. Format of 4th data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
LEV3	LEV2	LEV1	LEV0	CI3	CI2	CI1	0

Table 24. Description of 4th data byte bits

Bit	Symbol	Description
7 to 4	LEV[3:0]	level ADC output
3 to 1	CI[3:1]	<b>Chip Identification:</b> these bits have to be set to logic 0
0	-	this bit is internally set to logic 0

Table 25. Format of 5th data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
0	0	0	0	0	0	0	0

Table 26. Description of 5th data byte bits

Bit	Symbol	Description
7 to 0	-	reserved for future extensions; these bits are internally set to logic 0

9. Internal circuitry

Table 27. Internal circuitry

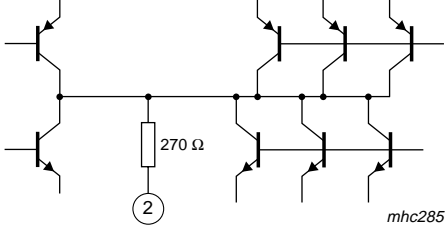
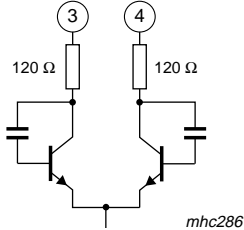
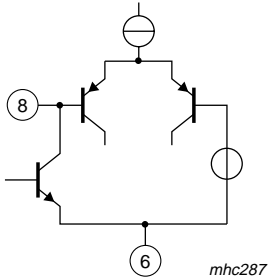
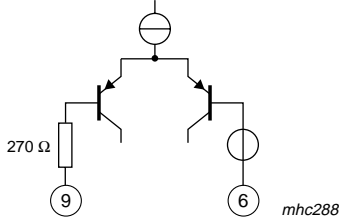
Pin	Symbol	Equivalent circuit
1	n.c.	
2	CPOUT	
3	$V_{COTANK1}$	
4	$V_{COTANK2}$	
5	$V_{CC(VCO)}$	
6	DGND	
7	$V_{CCD}$	
8	DATA	
9	CLOCK	
10	n.c.	

Table 27. Internal circuitry

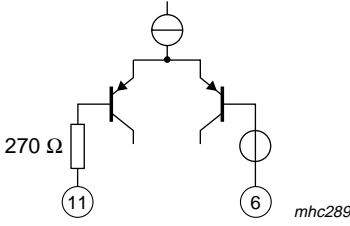
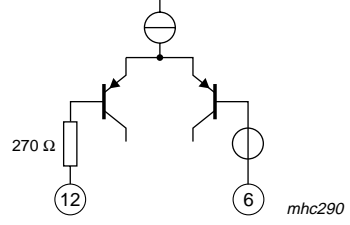
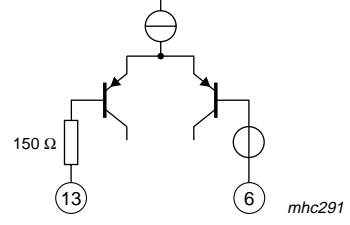
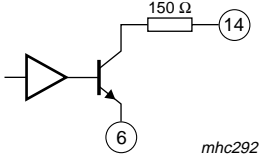
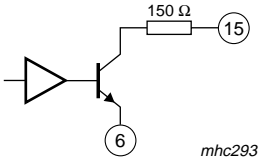
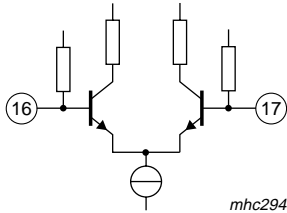
Pin	Symbol	Equivalent circuit
11	WRITE/READ	 <p><i>mhc289</i></p>
12	BUSMODE	 <p><i>mhc290</i></p>
13	BUSENABLE	 <p><i>mhc291</i></p>
14	SWPORT1	 <p><i>mhc292</i></p>
15	SWPORT2	 <p><i>mhc293</i></p>
16	XTAL1	 <p><i>mhc294</i></p>
17	XTAL2	

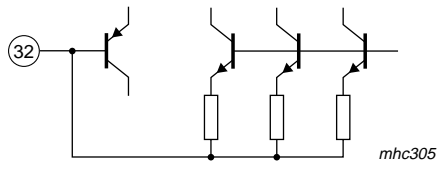
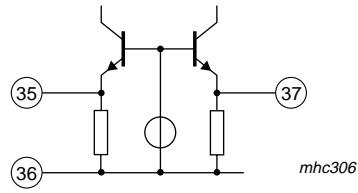
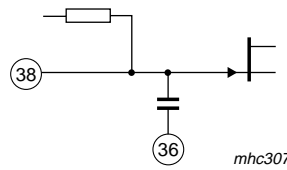
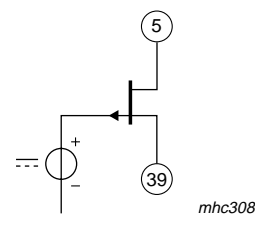
Table 27. Internal circuitry

Pin	Symbol	Equivalent circuit
18	PHASEFIL	<p>mhc295</p>
19	PILFIL	<p>mhc296</p>
20	n.c.	
21	n.c.	
22	V <sub>AFL</sub>	<p>mhc297</p>
23	V <sub>AFR</sub>	<p>mhc298</p>
24	TMUTE	<p>mhc299</p>

Table 27. Internal circuitry

Pin	Symbol	Equivalent circuit
25	MPXO	
26	$V_{ref}$	
27	TIFC	
28	LIMDEC1	
29	LIMDEC2	
30	n.c.	
31	n.c.	

Table 27. Internal circuitry

Pin	Symbol	Equivalent circuit
32	$I_{gain}$	 <p>mhc305</p>
33	AGND	
34	$V_{CCA}$	
35	RFI1	
36	RFGND	
37	RFI2	 <p>mhc306</p>
38	TAGC	 <p>mhc307</p>
39	LOOPSW	 <p>mhc308</p>
40	n.c.	

## 10. Limiting values

Table 28. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{VCOTANK1}$	VCO tuned circuit output voltage 1		-0.3	+8	V
$V_{VCOTANK2}$	VCO tuned circuit output voltage 2		-0.3	+8	V
$V_{CCD}$	digital supply voltage		-0.3	+5	V
$V_{CCA}$	analog supply voltage		-0.3	+8	V
$T_{stg}$	storage temperature		-55	+150	°C
$T_{amb}$	ambient temperature		-10	+75	°C

**Table 28. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{\text{esd}}$	electrostatic discharge voltage	all pins except pin DATA	[1]	-200	+200	V
			[2]	-2000	+2000	V
		pin DATA	[1]	-150	+200	V
			[2]	-2000	+2000	V

[1] Machine model (R = 0  $\Omega$ , C = 200 pF).[2] Human body model (R = 1.5 k $\Omega$ , C = 100 pF).

## 11. Thermal characteristics

**Table 29. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{\text{th(j-a)}}$	thermal resistance from junction to ambient	in free air	29	K/W

## 12. Static characteristics

**Table 30. Static characteristics** $V_{\text{CCA}} = V_{\text{CC(VCO)}} = V_{\text{CCD}} = 2.7 \text{ V}$ ;  $T_{\text{amb}} = 25^\circ\text{C}$ ; All AC values are given in RMS unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Supply voltages</b> [1]							
$V_{\text{CCA}}$	analog supply voltage		2.5	3.0	5.0	V	
$V_{\text{CC(VCO)}}$	VCO supply voltage		2.5	3.0	5.0	V	
$V_{\text{CCD}}$	digital supply voltage		2.5	3.0	5.0	V	
<b>Supply currents</b>							
$I_{\text{CCA}}$	analog supply current	operating					
		$V_{\text{CCA}} = 3 \text{ V}$	6.0	8.4	10.5	mA	
		$V_{\text{CCA}} = 5 \text{ V}$	6.2	8.6	10.7	mA	
		Standby mode					
		$V_{\text{CCA}} = 3 \text{ V}$	-	3	6	$\mu\text{A}$	
$I_{\text{CC(VCO)}}$	VCO supply current	operating					
		$V_{\text{CC(VCO)}} = 3 \text{ V}$	560	750	940	$\mu\text{A}$	
		$V_{\text{CC(VCO)}} = 5 \text{ V}$	570	760	950	$\mu\text{A}$	
		Standby mode					
		$V_{\text{CC(VCO)}} = 3 \text{ V}$	-	1	2	$\mu\text{A}$	
		$V_{\text{CC(VCO)}} = 5 \text{ V}$	-	1.2	2.2	$\mu\text{A}$	

**Table 30. Static characteristics ...continued**

$V_{CCA} = V_{CC(VCO)} = V_{CCD} = 2.7\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; All AC values are given in RMS unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CCD}$	digital supply current	operating				
		$V_{CCD} = 3\text{ V}$	2.1	3.0	3.9	mA
		$V_{CCD} = 5\text{ V}$	2.25	3.15	4.05	mA
		Standby mode; $V_{CCD} = 3\text{ V}$				
		bus enable line HIGH	30	56	80	$\mu\text{A}$
		bus enable line LOW	11	19	26	$\mu\text{A}$
		Standby mode; $V_{CCD} = 5\text{ V}$				
		bus enable line HIGH	50	78	105	$\mu\text{A}$
bus enable line LOW	20	33	45	$\mu\text{A}$		

[1]  $V_{CCA}$ ,  $V_{CC(VCO)}$  and  $V_{CCD}$  must not differ by more than 200 mV.

**Table 31. DC operating points, unloaded DC voltage**

$V_{CCA} = V_{CC(VCO)} = V_{CCD} = 2.7\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Operating point	Conditions	Min	Typ	Max	Unit
$V_{CPOUT}$		0.1	-	$V_{CC(VCO)} - 0.1$	V
$V_{XTAL2}$	data byte 4 bit 4 = 1	1.64	1.72	1.8	V
	data byte 4 bit 4 = 0	1.68	1.75	1.82	V
$V_{XTAL2}$	data byte 4 bit 4 = 1	1.64	1.72	1.8	V
	data byte 4 bit 4 = 0	1.68	1.75	1.82	V
$V_{PHASEFIL}$		0.4	1.2	$V_{CCA} - 0.4$	V
$V_{PILFIL}$		0.65	0.9	1.3	V
$V_{AFL}$	$f_{RF} = 98\text{ MHz}$ ; $V_{RF} = 1\text{ mV}$	720	850	940	mV
$V_{AFR}$	$f_{RF} = 98\text{ MHz}$ ; $V_{RF} = 1\text{ mV}$	720	850	940	mV
$V_{TMUTE}$	$V_{RF} = 0\text{ V}$	1.5	1.65	1.8	V
$V_{MPXO}$	$f_{RF} = 98\text{ MHz}$ ; $V_{RF} = 1\text{ mV}$	680	815	950	mV
$V_{ref}$		1.45	1.55	1.65	V
$V_{TIFC}$		1.34	1.44	1.54	V
$V_{LIMDEC1}$		1.86	1.98	2.1	V
$V_{LIMDEC2}$		1.86	1.98	2.1	V
$V_{Igain}$		480	530	580	mV
$V_{RF11}$		0.93	1.03	1.13	V
$V_{RF12}$		0.93	1.03	1.13	V
$V_{TAGC}$	$V_{RF} = 0\text{ V}$	1	1.57	2	V



### 13. Dynamic characteristics

**Table 32. Dynamic characteristics**

$V_{CCA} = V_{CCD} = V_{CC(VCO)} = 2.7\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; AC values given in RMS;  
For  $V_{RF}$  the emf value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>VCO</b>						
$f_{osc}$	oscillator frequency		150	-	217	MHz
<b>Crystal oscillator</b>						
Circuit input: pin XTAL2						
$V_{i(osc)}$	oscillator input voltage	oscillator externally clocked	140	-	350	mV
$R_i$	input resistance	oscillator externally clocked				
		data byte 4 bit 4 = 0	2	3	4	k $\Omega$
		data byte 4 bit 4 = 1	230	330	430	k $\Omega$
$C_i$	input capacitance	oscillator externally clocked				
		data byte 4 bit 4 = 0	3.9	5.6	7.3	pF
		data byte 4 bit 4 = 1	5	6	7	pF
<b>Crystal: 32.768 kHz</b>						
$f_r$	series resonance frequency	data byte 4 bit 4 = 1	-	32.768	-	kHz
$\Delta f/f_r$	frequency deviation		$-20 \times 10^{-6}$	-	$+20 \times 10^{-6}$	
$C_0$	shunt capacitance		-	-	3.5	pF
$R_S$	series resistance		-	-	80	k $\Omega$
$\Delta f_r/f_r(25\text{ °C})$	temperature drift	$-10\text{ °C} < T_{amb} < +60\text{ °C}$	$-50 \times 10^{-6}$	-	$+50 \times 10^{-6}$	
<b>Crystal: 13 MHz</b>						
$f_r$	series resonance frequency	data byte 4 bit 4 = 0	-	13	-	MHz
$\Delta f/f_r$	frequency deviation		$-30 \times 10^{-6}$	-	$+30 \times 10^{-6}$	
$C_0$	shunt capacitance		-	-	4.5	pF
$C_{mot}$	motional capacitance		1.5	-	3.0	fF
$R_S$	series resistance		-	-	100	k $\Omega$
$\Delta f_r/f_r(25\text{ °C})$	temperature drift	$-40\text{ °C} < T_{amb} < +85\text{ °C}$	$-30 \times 10^{-6}$	-	$+30 \times 10^{-6}$	
<b>Synthesizer</b>						
<b>Programmable divider<sup>[1]</sup></b>						
$N_{prog}$	programmable divider ratio	data byte 1 = XX11 1111; data byte 2 = 1111 1110	-	-	8191	-
		data byte 1 = XX01 0000; data byte 2 = 0000 0000	2048	-	-	-
$\Delta N_{step}$	programmable divider step size		-	1	-	-
<b>Reference frequency divider</b>						
$N_{ref}$	crystal oscillator divider ratio	data byte 4 bit 4 = 0	-	260	-	-
		data byte 5 bit 7 = 1; data byte 4 bit 4 = 0	-	130	-	-
		data byte 4 bit 4 = 1	-	1	-	-

**Table 32. Dynamic characteristics ...continued**

$V_{CCA} = V_{CCD} = V_{CC(VCO)} = 2.7\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; AC values given in RMS;  
For  $V_{RF}$  the emf value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Charge pump: pin CPOUT</b>						
$I_{sink}$	charge pump peak sink current	$0.2\text{ V} < V_{CPOUT} < V_{VCOTANK2} - 0.2\text{ V}$ ; $f_{VCO} > f_{ref} \times N_{prog}$	-	0.5	-	$\mu\text{A}$
$I_{source}$	charge pump peak source current	$0.2\text{ V} < V_{CPOUT} < V_{VCOTANK2} - 0.2\text{ V}$ ; $f_{VCO} < f_{ref} \times N_{prog}$	-	-0.5	-	$\mu\text{A}$
<b>IF counter</b>						
$V_{RF}$	RF input voltage for correct IF count		-	12	18	$\mu\text{V}$
$N_{IF}$	IF counter length		-	7	-	bit
$N_{precount}$	IF counter prescaler ratio		-	64	-	-
$T_{count(IF)}$	IF counter period	$f_{xtal} = 32.768\text{ kHz}$	-	15.625	-	ms
		$f_{xtal} = 13\text{ MHz}$	-	15.754	-	ms
$RES_{count(IF)}$	IF counter resolution	$f_{xtal} = 32.768\text{ kHz}$	-	4.096	-	kHz
		$f_{xtal} = 13\text{ MHz}$	-	4.0625	-	kHz
$IF_{count}$	IF counter result for search tuning stop	$f_{xtal} = 32.768\text{ kHz}$	29h	-	3Dh	-
		$f_{xtal} = 13\text{ MHz}$	30h	-	3Dh	-
<b>Pins DATA, CLOCK, WRITE/READ, BUSMODE and BUSENABLE</b>						
$R_i$	input resistance		10	-	-	$\text{M}\Omega$

**Table 32. Dynamic characteristics ...continued**

$V_{CCA} = V_{CCD} = V_{CC(VCO)} = 2.7\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; AC values given in RMS;  
For  $V_{RF}$  the emf value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Software programmable ports</b>						
<b>Pin SWPORT1</b>						
$I_{\text{sink(max)}}$	maximum sink current	data byte 3 bit 0 = 0; data byte 4 bit 0 = 0; $V_{\text{SWPORT1}} < 0.5\text{ V}$	500	-	-	$\mu\text{A}$
$I_{\text{leak(max)}}$	maximum leakage current	data byte 3 bit 0 = 1; $V_{\text{SWPORT1}} < 5\text{ V}$	-1	-	+1	$\mu\text{A}$
<b>Pin SWPORT2</b>						
$I_{\text{sink(max)}}$	maximum sink current	data byte 4 bit 7 = 0; $V_{\text{SWPORT1}} < 0.5\text{ V}$	500	-	-	$\mu\text{A}$
$I_{\text{leak(max)}}$	maximum leakage current	data byte 4 bit 7 = 1; $V_{\text{SWPORT1}} < 5\text{ V}$	-1	-	+1	$\mu\text{A}$
<b>FM signal channel</b>						
<b>FM RF input</b>						
$f_{\text{FM(ant)}}$	FM input frequency		76	-	108	MHz
$R_i$	input resistance at pins RFI1 and RFI2 to RFGND		75	100	125	$\Omega$
$C_i$	input capacitance at pins RFI1 and RFI2 to RFGND		2.5	4	6	pF
$V_{\text{RF}}$	RF sensitivity input voltage	$f_{\text{RF}} = 76\text{ MHz to }108\text{ MHz}$ ; $\Delta f = 22.5\text{ kHz}$ ; $f_{\text{mod}} = 1\text{ kHz}$ ; (S+N)/N = 26 dB; L = R; de-emphasis = 75 $\mu\text{s}$ ; $B_{\text{AF}} = 300\text{ Hz to }15\text{ kHz}$	-	2	3.5	$\mu\text{V}$
$\text{IP3}_{\text{in}}$	in-band 3rd-order intercept point related to $V_{\text{RFI1-RFI2}}$ (peak value)	$\Delta f_1 = 200\text{ kHz}$ ; $\Delta f_2 = 400\text{ kHz}$ ; $f_{\text{tune}} = 76\text{ MHz to }108\text{ MHz}$	81	84	-	$\text{dB}\mu\text{V}$
$\text{IP3}_{\text{out}}$	out-band 3rd-order intercept point related to $V_{\text{RFI1-RFI2}}$ (peak value)	$\Delta f_1 = 4\text{ MHz}$ ; $\Delta f_2 = 8\text{ Hz}$ ; $f_{\text{tune}} = 76\text{ MHz to }108\text{ MHz}$	82	85	-	$\text{dB}\mu\text{V}$
<b>RF AGC</b>						
$V_{\text{RF1}}$	RF input voltage for start of AGC	$f_{\text{RF1}} = 93\text{ MHz}$ ; $f_{\text{RF2}} = 98\text{ MHz}$ ; $V_{\text{RF2}} = 50\text{ dB}\mu\text{V}$ ; $\left  \frac{\Delta V_{\text{TMUTE}}}{V_{\text{RF1}}} \right  < \frac{14\text{ mV}}{3\text{ dB}\mu\text{V}}$	2] 66	72	78	$\text{dB}\mu\text{V}$
<b>IF filter</b>						
$f_{\text{IF}}$	IF filter center frequency		215	225	235	kHz
$B_{\text{IF}}$	IF filter bandwidth		85	94	102	kHz
$S_{+200}$	high side 200 kHz selectivity	$\Delta f = +200\text{ kHz}$ ; $f_{\text{tune}} = 76\text{ MHz to }108\text{ MHz}$	3] 39	43	-	dB
$S_{-200}$	low side 200 kHz selectivity	$\Delta f = -200\text{ kHz}$ ; $f_{\text{tune}} = 76\text{ MHz to }108\text{ MHz}$	3] 32	36	-	dB
$S_{+100}$	high side 100 kHz selectivity	$\Delta f = +100\text{ kHz}$ ; $f_{\text{tune}} = 76\text{ MHz to }108\text{ MHz}$	3] 8	12	-	dB

**Table 32. Dynamic characteristics ...continued**

$V_{CCA} = V_{CCD} = V_{CC(VCO)} = 2.7\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; AC values given in RMS;  
For  $V_{RF}$  the emf value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S <sub>-100</sub>	low side 100 kHz selectivity	$\Delta f = -100\text{ kHz}$ ; $f_{\text{tune}} = 76\text{ MHz to }108\text{ MHz}$	[3] 8	12	-	dB
IR	image rejection	$f_{\text{tune}} = 76\text{ MHz to }108\text{ MHz}$ ; $V_{RF} = 50\text{ dB}\mu\text{V}$	24	30	-	dB
<b>FM IF level detector and mute voltage</b>						
$V_{RF}$	RF input voltage for start of level ADC	read mode data byte 4 bit 4 = 1	2	3	5	$\mu\text{V}$
$\Delta V_{\text{step}}$	level ADC step size		2	3	5	dB
<b>Pin TMUTE</b>						
$V_{\text{level}}$	level output DC voltage	$V_{RF} = 0\text{ }\mu\text{V}$	1.55	1.65	1.80	V
		$V_{RF} = 3\text{ }\mu\text{V}$	1.60	1.70	1.85	V
$V_{\text{level(slope)}}$	slope of level voltage	$V_{RF} = 10\text{ }\mu\text{V to }500\text{ }\mu\text{V}$	150	165	180	$\frac{\text{mV}}{20\text{ dB}}$
$R_o$	output resistance		280	400	520	k $\Omega$
<b>FM demodulator: pin MPXO</b>						
$V_{\text{MPXO}}$	demodulator output voltage	$V_{RF} = 1\text{ mV}$ ; L = R; $\Delta f = 22.5\text{ kHz}$ ; $f_{\text{mod}} = 1\text{ kHz}$ ; de-emphasis = 75 $\mu\text{s}$ ; $B_{AF} = 300\text{ Hz to }15\text{ kHz}$	60	75	90	mV
(S+N)/N	maximum signal plus noise-to-noise ratio	$V_{RF} = 1\text{ mV}$ ; L = R; $\Delta f = 22.5\text{ kHz}$ ; $f_{\text{mod}} = 1\text{ kHz}$ ; de-emphasis = 75 $\mu\text{s}$ ; $B_{AF} = 300\text{ Hz to }15\text{ kHz}$	54	60	-	dB
THD	total harmonic distortion	$V_{RF} = 1\text{ mV}$ ; L = R; $\Delta f = 75\text{ kHz}$ ; $f_{\text{mod}} = 1\text{ kHz}$ ; de-emphasis = 75 $\mu\text{s}$	-	0.5	1.5	%
$\alpha_{AM}$	AM suppression	$V_{RF} = 300\text{ }\mu\text{V}$ ; L = R; $\Delta f = 22.5\text{ kHz}$ ; $f_{\text{mod}} = 1\text{ kHz}$ ; $m = 0.3$ ; de-emphasis = 75 $\mu\text{s}$ ; $B_{AF} = 300\text{ Hz to }15\text{ kHz}$	40	-	-	dB
$R_o$	demodulator output resistance		-	-	500	$\Omega$
$I_{\text{sink}}$	demodulator output sink current		-	-	30	$\mu\text{A}$
<b>Soft mute</b>						
$V_{RF}$	RF input voltage for soft mute start	$\alpha_{\text{mute}} = 3\text{ dB}$ ; data byte 4 bit 3 = 1	3	5	10	$\mu\text{V}$
$\alpha_{\text{mute}}$	mute attenuation	$V_{RF} = 1\text{ }\mu\text{V}$ ; L = R; $\Delta f = 22.5\text{ kHz}$ ; $f_{\text{mod}} = 1\text{ kHz}$ ; de-emphasis = 75 $\mu\text{s}$ ; $B_{AF} = 300\text{ Hz to }15\text{ kHz}$ ; data byte 4 bit 3 = 1	4	7	15	dB

**Table 32. Dynamic characteristics ...continued**

$V_{CCA} = V_{CCD} = V_{CC(VCO)} = 2.7\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; AC values given in RMS;  
For  $V_{RF}$  the emf value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>MPX decoder</b>						
$V_{AFL}$	left audio frequency output voltage	$V_{RF} = 1\text{ mV}$ ; $L = R$ ; $\Delta f = 22.5\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; de-emphasis = $75\text{ }\mu\text{s}$	60	75	90	mV
$V_{AFR}$	right audio frequency output voltage	$V_{RF} = 1\text{ mV}$ ; $L = R$ ; $\Delta f = 22.5\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; de-emphasis = $75\text{ }\mu\text{s}$	60	75	90	mV
$R_{AFL}$	left audio frequency output resistance		-	-	50	$\Omega$
$R_{AFR}$	right audio frequency output resistance		-	-	50	$\Omega$
$I_{sink(AFL)}$	left audio frequency output sink current		170	-	-	$\mu\text{A}$
$I_{sink(AFR)}$	right audio frequency output sink current		170	-	-	$\mu\text{A}$
$V_{MPXIN(max)}$	input overdrive margin	THD < 3 %	4	-	-	dB
$V_{AFL}$	left audio frequency output voltage difference	$V_{RF} = 1\text{ mV}$ ; $L = R$ ; $\Delta f = 75\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; de-emphasis = $75\text{ }\mu\text{s}$	-1	-	+1	dB
$V_{AFR}$	right audio frequency output voltage difference	$V_{RF} = 1\text{ mV}$ ; $L = R$ ; $\Delta f = 75\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; de-emphasis = $75\text{ }\mu\text{s}$	-1	-	+1	dB
$\alpha_{cs(stereo)}$	stereo channel separation	$V_{RF} = 1\text{ mV}$ ; $R = L = 0$ or $R = 0$ and $L = 1$ including 9 % pilot; $\Delta f = 75\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; data byte 3 bit 3 = 0; data byte 4 bit 1 = 1	24	30	-	dB
(S+N)/N	maximum signal plus noise-to-noise ratio	$V_{RF} = 1\text{ mV}$ ; $L = R$ ; $\Delta f = 22.5\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; de-emphasis = $75\text{ }\mu\text{s}$ ; $B_{AF} = 300\text{ Hz to }15\text{ kHz}$	54	60	-	dB
THD	total harmonic distortion	$V_{RF} = 1\text{ mV}$ ; $L = R$ ; $\Delta f = 75\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; de-emphasis = $75\text{ }\mu\text{s}$	-	0.4	1	%
$\alpha_{pilot}$	pilot suppression measured at pins $V_{AFL}$ and $V_{AFR}$	related to $\Delta f = 75\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; de-emphasis = $75\text{ }\mu\text{s}$	40	50	-	dB
$\Delta f_{pilot}$	stereo pilot frequency deviation	$V_{RF} = 1\text{ mV}$ ; read mode data byte 3 bit 7 = 1	-	3.6	5.8	kHz
		data byte 3 bit 7 = 0	1	3	-	kHz
$\frac{\Delta f_{pilot1}}{\Delta f_{pilot2}}$	pilot switch hysteresis	$V_{RF} = 1\text{ mV}$	2	-	-	dB

**Table 32. Dynamic characteristics ...continued**

$V_{CCA} = V_{CCD} = V_{CC(VCO)} = 2.7\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; AC values given in RMS;  
For  $V_{RF}$  the emf value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>High cut control</b>						
TC <sub>de-em</sub>	de-emphasis time constant	$V_{RF} = 1\text{ mV}$				
		data byte 5 bit 6 = 0	38	50	62	μs
		data byte 5 bit 6 = 1	57	75	93	μs
		$V_{RF} = 1\text{ }μ\text{V}$				
		data byte 5 bit 6 = 0	114	150	186	μs
		data byte 5 bit 6 = 1	171	225	279	μs
<b>Mono to stereo blend control</b>						
$\alpha_{cs(\text{stereo})}$	stereo channel separation	$V_{RF} = 45\text{ }μ\text{V}$ ; R = L = 0 or R = 0 and L = 1 including 9 % pilot; $\Delta f = 75\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; data byte 3 bit 3 = 0; data byte 4 bit 1 = 1	4	10	16	dB
<b>Mono to stereo switched</b>						
$\alpha_{cs(\text{stereo})}$	stereo channel separation switching from mono to stereo with increasing RF input level	R = L = 0 or R = 0 and L = 1 including 9 % pilot; $\Delta f = 75\text{ kHz}$ ; $f_{mod} = 1\text{ kHz}$ ; data byte 3 bit 3 = 0; data byte 4 bit 1 = 0				
		$V_{RF} = 1\text{ mV}$	24	-	-	dB
		$V_{RF} = 20\text{ }μ\text{V}$	-	-	1	dB
<b>Bus-driven mute functions</b>						
<b>Tuning mute</b>						
$\alpha_{mute}$	$V_{AFL}$ and $V_{AFR}$ muting depth	data byte 1 bit 7 = 1	-	-	-60	dB
$\alpha_{mute(L)}$	$V_{AFL}$ muting depth	data byte 3 bit 1 = 1; $f_{AF} = 1\text{ kHz}$ ; $R_{load(L)} < 30\text{ k}\Omega$	-	-	-80	dB
$\alpha_{mute(R)}$	$V_{AFR}$ muting depth	data byte 3 bit 2 = 1; $f_{AF} = 1\text{ kHz}$ ; $R_{load(R)} < 30\text{ k}\Omega$	-	-	-80	dB

[1] Calculation of this 14-bit word can be done as follows:

$$\text{formula for high side injection: } N = \frac{4 \times (f_{RF} + f_{IF})}{f_{ref}}; \text{ formula for low side injection: } N = \frac{4 \times (f_{RF} - f_{IF})}{f_{ref}}$$

where:

N = decimal value of PLL word;

$f_{RF}$  = the wanted tuning frequency [Hz];

$f_{IF}$  = the intermediate frequency [Hz] = 225 kHz;

$f_{ref}$  = the reference frequency [Hz] = 32.768 kHz for the 32.768 kHz crystal;  $f_{ref} = 50\text{ kHz}$  for the 13 MHz crystal or when externally clocked with 6.5 MHz.

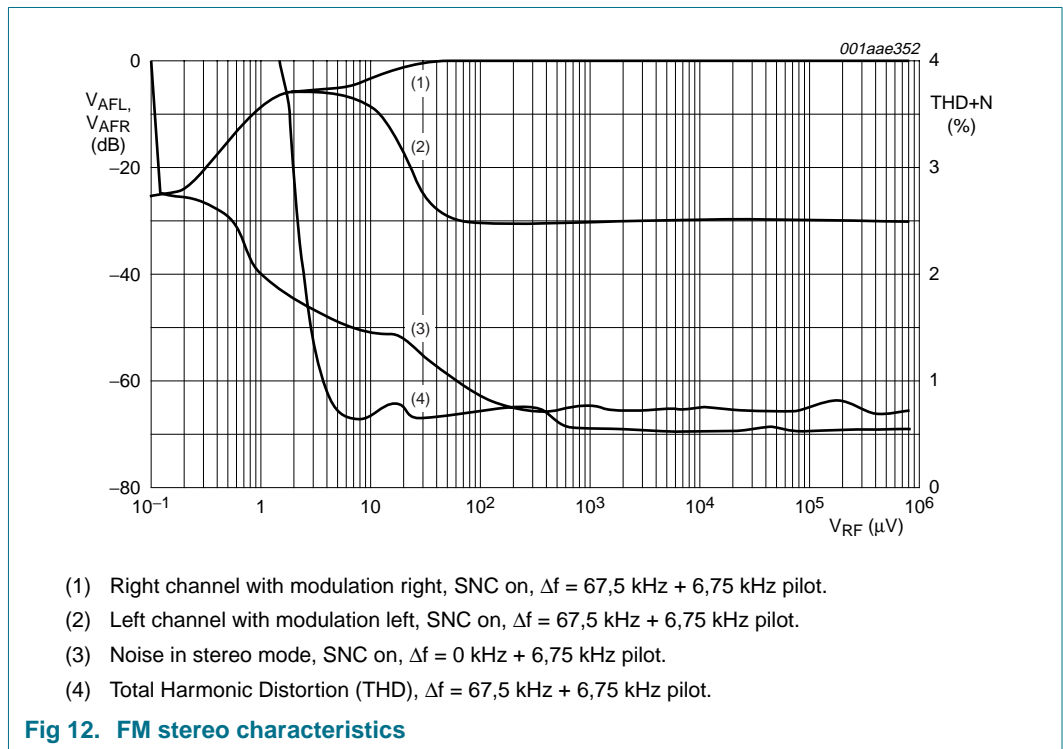
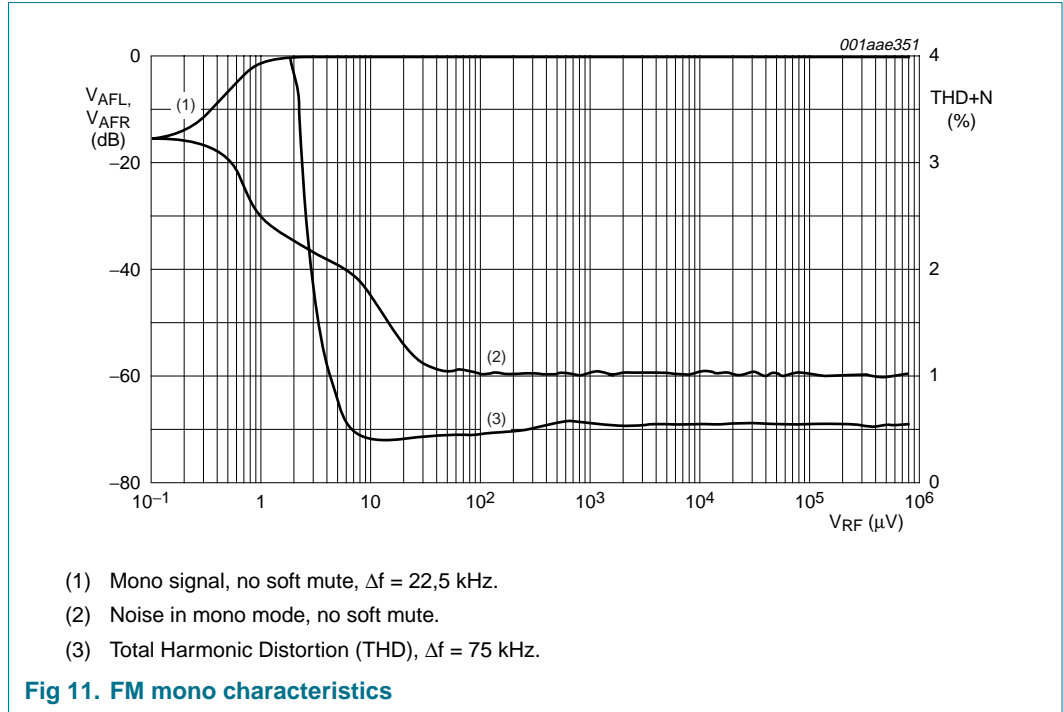
$$\text{Example for receiving a channel at } 100\text{ MHz with high side injection: } N = \frac{4 \times (100 \times 10^6 + 225 \times 10^3)}{32768} = 12234$$

The PLL word becomes 2FCAh.

[2]  $V_{RF}$  in [Figure 13](#) is replaced by  $V_{RF1} + V_{RF2}$ . The radio is tuned to 98 MHz (high side injection).

[3] Low side and high side selectivity can be switched by changing the mixer from high side to low side LO injection.

14. FM characteristics



## 15. I<sup>2</sup>C-bus characteristics

Table 33. Digital levels and timing

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Digital inputs</b>					
V <sub>IH</sub>	HIGH-level input voltage		0.45V <sub>CCD</sub>	-	V
V <sub>IL</sub>	LOW-level input voltage		-	0.2V <sub>CCD</sub>	V
<b>Digital outputs</b>					
I <sub>sink(L)</sub>	LOW-level sink current		500	-	μA
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 500 μA	-	450	mV
<b>Timing</b>					
f <sub>clk</sub>	clock input frequency	I <sup>2</sup> C-bus enabled	-	400	kHz
		3-wire bus enabled	-	400	kHz
t <sub>HIGH</sub>	clock HIGH time	I <sup>2</sup> C-bus enabled	1	-	μs
		3-wire bus enabled	1	-	μs
t <sub>LOW</sub>	clock LOW time	I <sup>2</sup> C-bus enabled	1	-	μs
		3-wire bus enabled	1	-	μs
t <sub>W(write)</sub>	pulse width for write enable	3-wire bus enabled	1	-	μs
t <sub>W(read)</sub>	pulse width for read enable	3-wire bus enabled	1	-	μs
t <sub>SU(clk)</sub>	clock set-up time	3-wire bus enabled	300	-	ns
t <sub>h(out)</sub>	read mode data output hold time	3-wire bus enabled	10	-	ns
t <sub>d(out)</sub>	read mode output delay time	3-wire bus enabled	-	400	ns
t <sub>SU(write)</sub>	write mode set-up time	3-wire bus enabled	100	-	ns
t <sub>h(write)</sub>	write mode hold time	3-wire bus enabled	100	-	ns

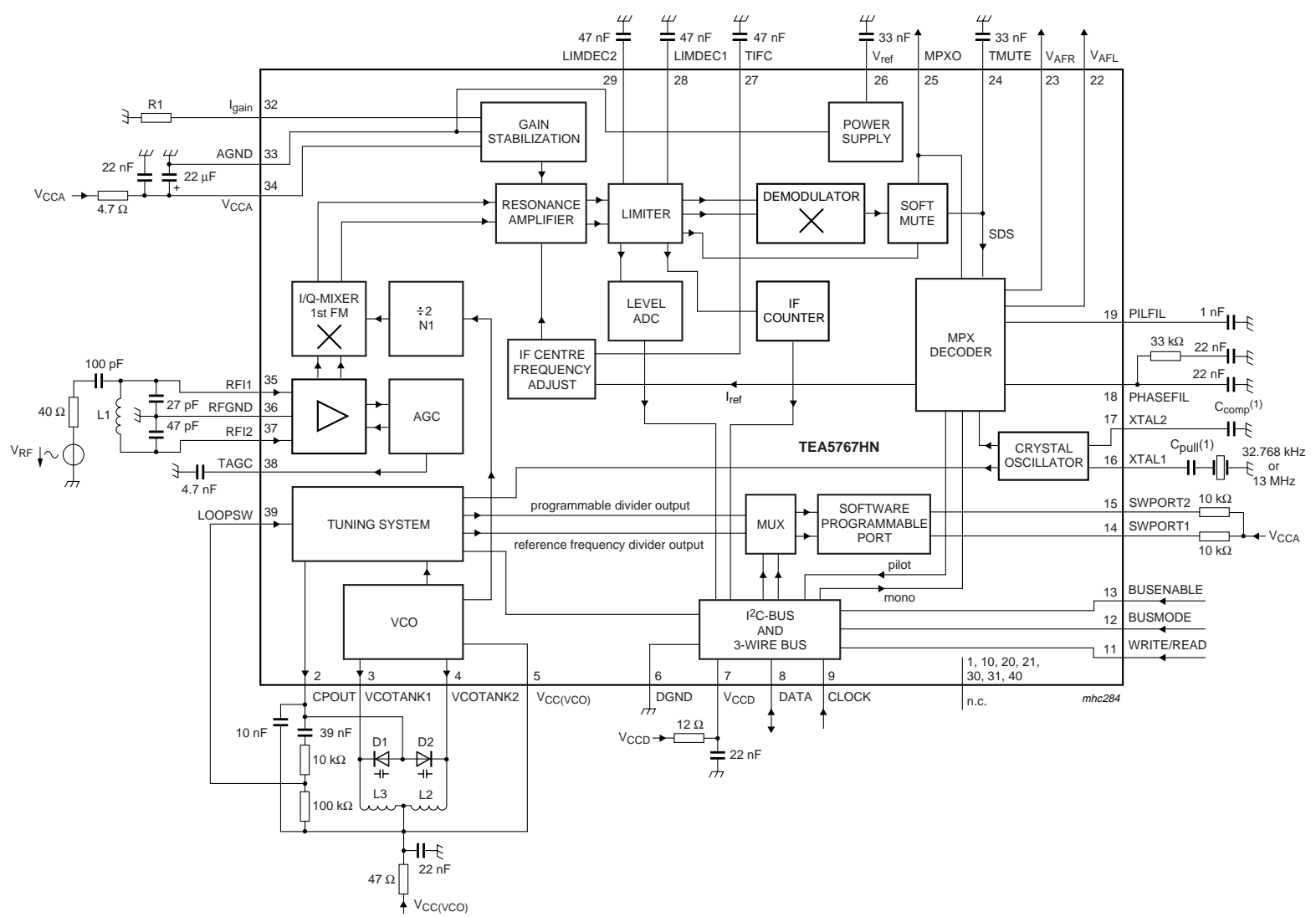
## 16. Test information

Table 34. Component list for [Figure 1](#) and [Figure 13](#)

Component	Parameter	Value	Tolerance	Type	Manufacturer
R1	resistor with low temperature coefficient	18 kΩ	±1 %	RC12G	Philips
D1 and D2	varicap for VCO tuning	-	-	BB202	Philips
L1	RF band filter coil	120 nH	±2 %	Q <sub>min</sub> = 40	
L2 and L3	VCO coil	33 nH	±2 %	Q <sub>min</sub> = 40	
XTAL13MHz	13 MHz crystal	-	-	NX4025GA	
C <sub>pull</sub>	pulling capacitor for NX4025GA	10 pF	-		
XTAL32768Hz	32,768 kHz crystal	-	-		
C <sub>pull</sub>	pulling capacitor for XTAL32768Hz	C <sub>load</sub> <sup>[1]</sup>	-		

[1] Value of the C<sub>pull</sub> must be as close as possible to the value of C<sub>load</sub> of the crystal.





Value of  $C_{pull}$  must be as close as possible to the value of  $C_{load}$  of the crystal.

(1)  $C_{comp}$  and  $C_{pull}$  data depends on crystal specification.

Fig 13. Application and test diagram

17. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm

SOT618-1

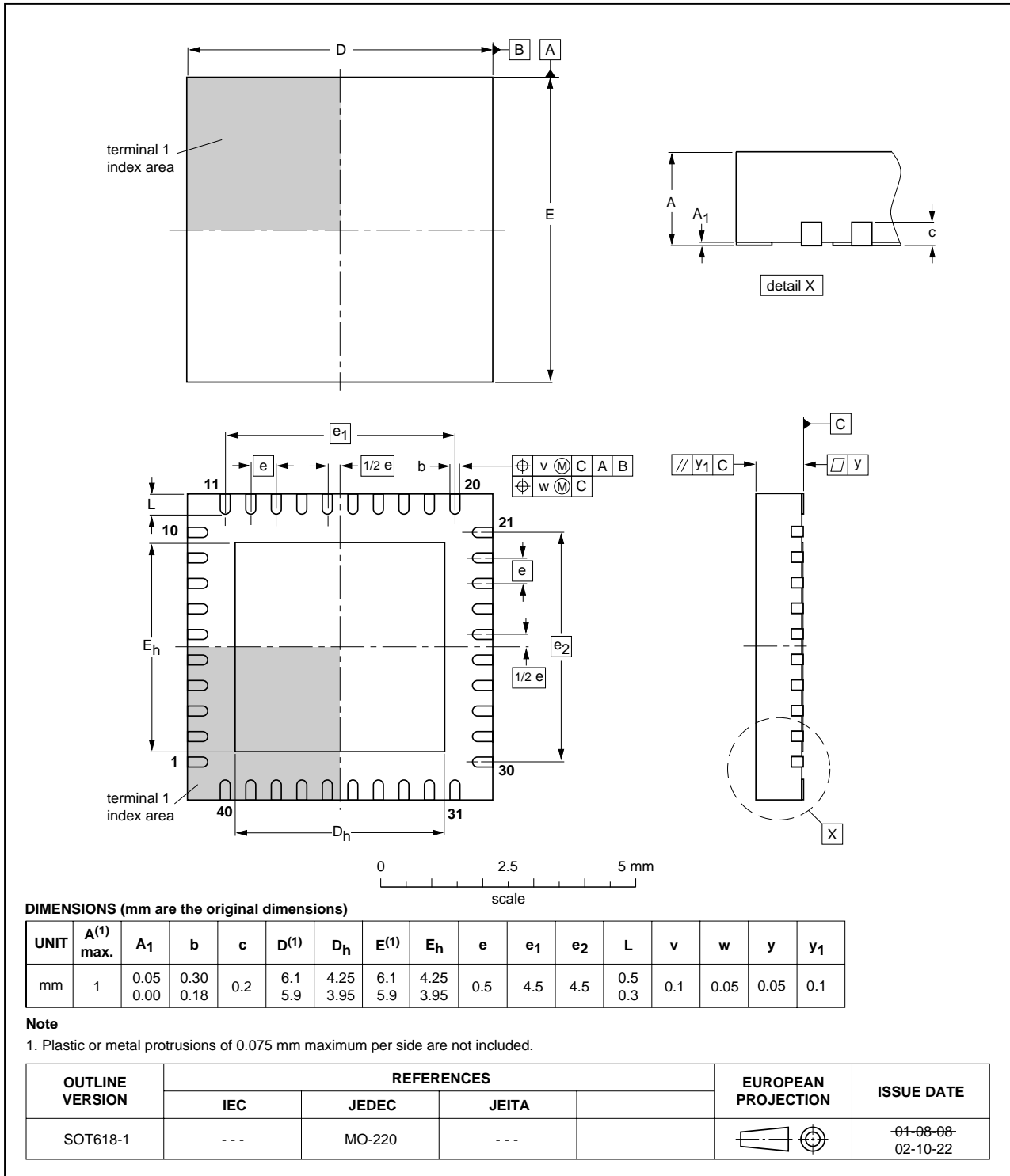


Fig 14. Package outline SOT618-1 (HVQFN40)

## 18. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

### 18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 15](#)) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 35](#) and [36](#)

**Table 35. SnPb eutectic process (from J-STD-020C)**

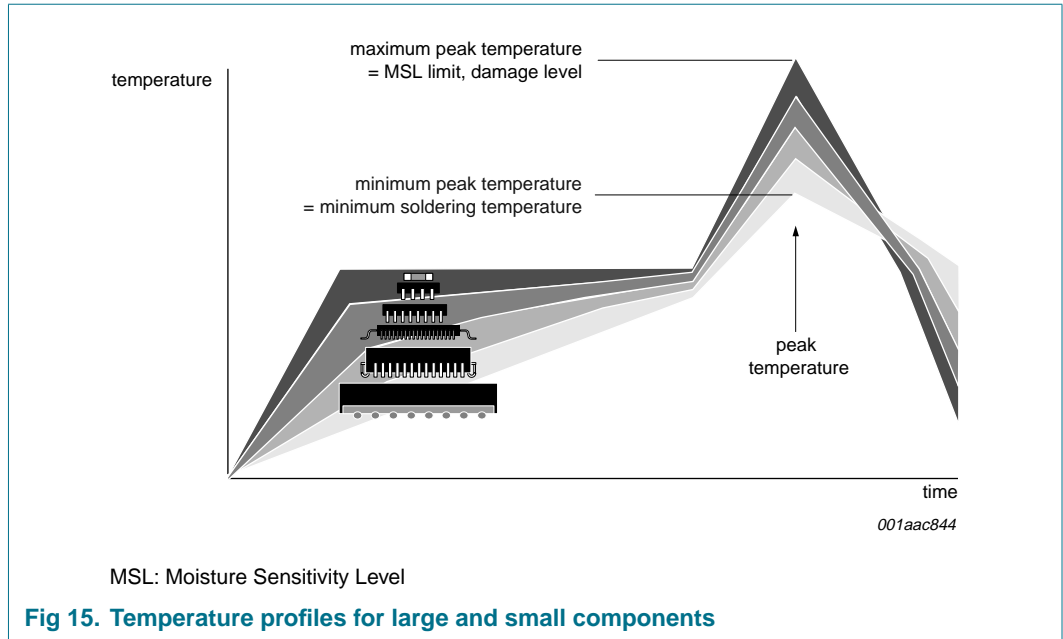
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 36. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 15](#).



For further information on temperature profiles, refer to Application Note AN10365 "Surface mount reflow soldering description".

## 19. Revision history

Table 37. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA5767HN_5	20070126	Product data sheet	-	TEA5767HN_4
Modifications:	<ul style="list-style-type: none"> <li>Modified: <a href="#">Section 13 "Dynamic characteristics"</a> values of Soft mute, mute attenuation are changed</li> </ul>			
TEA5767HN_4	20060220	Product data sheet	-	TEA5767HN_3 (9397 750 13531)
TEA5767HN_3 (9397 750 13531)	20040920	Product specification	-	TEA5767HN_2 (9397 750 12071)
TEA5767HN_2 (9397 750 12071)	20031112	Preliminary specification	-	TEA5767HN_1 (9397 750 09626)
TEA5767HN_1 (9397 750 09626)	20020913	Preliminary specification	-	-

## 20. Legal information

### 20.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 20.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 20.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to

result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**I<sup>2</sup>C-bus** — logo is a trademark of NXP B.V.

## 21. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

22. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>	<b>17</b>	<b>Package outline</b> .....	<b>34</b>
<b>2</b>	<b>Features</b> .....	<b>1</b>	<b>18</b>	<b>Soldering</b> .....	<b>35</b>
<b>3</b>	<b>Quick reference data</b> .....	<b>2</b>	18.1	Introduction to soldering .....	35
<b>4</b>	<b>Ordering information</b> .....	<b>3</b>	18.2	Wave and reflow soldering .....	35
<b>5</b>	<b>Block diagram</b> .....	<b>4</b>	18.3	Wave soldering .....	35
<b>6</b>	<b>Pinning information</b> .....	<b>5</b>	18.4	Reflow soldering .....	36
6.1	Pinning .....	5	<b>19</b>	<b>Revision history</b> .....	<b>38</b>
6.2	Pin description .....	5	<b>20</b>	<b>Legal information</b> .....	<b>39</b>
<b>7</b>	<b>Functional description</b> .....	<b>6</b>	20.1	Data sheet status .....	39
7.1	Low-noise RF amplifier .....	6	20.2	Definitions .....	39
7.2	FM mixer .....	6	20.3	Disclaimers .....	39
7.3	VCO .....	6	20.4	Trademarks .....	39
7.4	Crystal oscillator .....	7	<b>21</b>	<b>Contact information</b> .....	<b>39</b>
7.5	PLL tuning system .....	7	<b>22</b>	<b>Contents</b> .....	<b>40</b>
7.6	RF AGC .....	7			
7.7	IF filter .....	7			
7.8	FM demodulator .....	7			
7.9	Level voltage generator and analog-to-digital converter .....	7			
7.10	IF counter .....	7			
7.11	Soft mute .....	7			
7.12	MPX decoder .....	7			
7.13	Signal dependent mono to stereo blend .....	8			
7.14	Signal dependent AF response .....	8			
7.15	Software programmable ports .....	8			
7.16	I <sup>2</sup> C-bus and 3-wire bus .....	8			
<b>8</b>	<b>I<sup>2</sup>C-bus, 3-wire bus and bus-controlled functions</b> .....	<b>10</b>			
8.1	I <sup>2</sup> C-bus specification .....	10			
8.1.1	Data transfer .....	10			
8.1.2	Power-on reset .....	11			
8.2	I <sup>2</sup> C-bus protocol .....	11			
8.3	3-wire bus specification .....	12			
8.3.1	Data transfer .....	12			
8.3.2	Power-on reset .....	13			
8.4	Writing data .....	13			
8.5	Reading data .....	16			
<b>9</b>	<b>Internal circuitry</b> .....	<b>18</b>			
<b>10</b>	<b>Limiting values</b> .....	<b>22</b>			
<b>11</b>	<b>Thermal characteristics</b> .....	<b>23</b>			
<b>12</b>	<b>Static characteristics</b> .....	<b>23</b>			
<b>13</b>	<b>Dynamic characteristics</b> .....	<b>25</b>			
<b>14</b>	<b>FM characteristics</b> .....	<b>31</b>			
<b>15</b>	<b>I<sup>2</sup>C-bus characteristics</b> .....	<b>32</b>			
<b>16</b>	<b>Test information</b> .....	<b>32</b>			

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2007.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 26 January 2007

Document identifier: TEA5767HN\_5